CLAIMS

What is claimed is:

1. A process for reconstructing a semiconductor wafer, comprising:

forming at least a first alignment droplet and at least a second alignment droplet from a flowable alignment material at laterally spaced locations on a substrate;

placing a first semiconductor die having at least one alignment cavity on a surface thereof, such that the at least one alignment cavity of the first semiconductor die makes contact with the at least a first alignment droplet and is positioned by surface tension thereof;

placing a second semiconductor die having at least one alignment cavity on a surface thereof, such that the at least one alignment cavity of the second semiconductor die makes contact with the at least a second alignment droplet and is positioned by surface tension thereof;

inducing the at least a first alignment droplet and the at least a second alignment droplet to at least partially solidify to maintain positions of the first semiconductor die and the second semiconductor die; and

introducing an underfill material adjacent the surfaces of the first and second semiconductor dice and surrounding the at least a first alignment droplet and the at least a second alignment droplet to form a reconstructed semiconductor wafer.

2. The process according to claim 1, wherein forming at least a first alignment droplet and at least a second alignment droplet from a flowable alignment material comprises extruding the flowable alignment material through at least a first alignment via and at least a second alignment via to form the at least a first alignment droplet and the at least a second alignment droplet.

3. The process according to claim 2, wherein extruding the flowable alignment material through at least a first alignment via and at least a second alignment via to form at least a first alignment droplet and at least a second alignment droplet comprises extruding the alignment material from a supply of alignment material operably coupled to a reconstruction table.

4. The process according to claim 2, wherein the substrate comprises a fixture plate and wherein extruding the flowable alignment material through at least a first alignment via and at least a second alignment via to form at least a first alignment droplet and at least a second alignment droplet comprises extruding the flowable alignment material through alignment vias located in the fixture plate to form part of the reconstructed semiconductor wafer.

5. The process according to claim 1, wherein inducing the at least a first alignment droplet and the at least a second alignment droplet to at least partially solidify and maintain the positions of the first semiconductor die and the second semiconductor die comprises at least one of raising or lowering a temperature of the alignment material to at least partially solidify the alignment droplets.

6. The process according to claim 1, wherein inducing the at least a first alignment droplet and the at least a second alignment droplet to at least partially solidify and maintain the positions of the first semiconductor die and the second semiconductor die comprises reacting the alignment material with an activating agent to at least partially solidify the alignment droplets.

7. The process according to claim 1, wherein placing a first semiconductor die having at least one alignment cavity on a surface thereof, such that the at least one alignment cavity of the first semiconductor die makes contact with the at least a first alignment droplet and is positioned by the surface tension thereof comprises placing a semiconductor die having a plurality of alignment cavities on a surface thereof, each of the alignment cavities interacting with a correspondingly positioned alignment droplet to position the semiconductor die.

8. The process according to claim 7, wherein placing a semiconductor die having a plurality of alignment cavities on a surface thereof comprises placing a semiconductor die having a grid pattern of alignment cavities.

9. The process according to claim 1, wherein introducing an underfill material adjacent the surfaces of the first and second semiconductor dice and surrounding the at least a first alignment droplet and the at least a second alignment droplet comprises introducing the underfill material between the first and second semiconductor dice and the substrate in the form of a fixture plate.

10. The process according to claim 1, further comprising curing the underfill material to a substantially solid state.

11. The process according to claim 1, further comprising singulating the first semiconductor die and the second semiconductor die from the reconstructed semiconductor wafer.

12. The process according to claim 11, wherein singulating the first semiconductor die and the second semiconductor die from the reconstructed semiconductor wafer comprises back-grinding the reconstructed semiconductor wafer to remove the underfill material.

13. The process according to claim 12, wherein back-grinding the reconstructed semiconductor wafer to remove the underfill material further comprises removing a fixture plate adhered to the underfill material by back-grinding the reconstructed semiconductor wafer.

14. The process according to claim 12, further comprising adhering active surfaces of the first semiconductor die and the second semiconductor die to an adhesive-coated film before singulating.

15. The process according to claim 14, further comprising removing the adhesive-coated film following the back-grinding.

16. A process for forming interconnective structures on a semiconductor die, the process comprising:

forming at least a first alignment droplet from a flowable alignment material;

placing a semiconductor die having at least one alignment cavity on a rear surface thereof, such that the at least one alignment cavity makes contact with the at least a first alignment droplet and is positioned by surface tension thereof;

inducing the at least a first alignment droplet to at least partially solidify and maintain a position of the semiconductor die;

introducing an underfill material adjacent the rear surface of the semiconductor die and surrounding the at least a first alignment droplet;

removing the alignment material from the surrounding underfill material to create at least one interconnect void adjacent the at least one alignment cavity;

filling the at least one interconnect void with an interconnect material to form at least one interconnect structure.

17. The process according to claim 16, further comprising removing the underfill material to substantially expose the at least one interconnect structure.

18. The process according to claim 16, wherein the at least one alignment cavity passes through an entire depth of the semiconductor die.

19. The process according to claim 18, wherein placing a semiconductor die having at least one alignment cavity on a rear surface thereof comprises placing a semiconductor die having at least one alignment cavity that substantially extends to an active surface of the semiconductor die.

20. The process according to claim 19, wherein placing a semiconductor die having at least one alignment cavity that substantially extends to an active surface of the semiconductor die comprises placing a semiconductor die where at least one alignment cavity is at least partially filled with a filler material.

21. The process according to claim 20, wherein placing a semiconductor die where at least one alignment cavity is at least partially filled with a filler material comprises placing a semiconductor die where at least one alignment cavity is at least partially filled with an electrically conductive filler material.

22. The process according to claim 21, further comprising removing the filler material from the at least one alignment cavity as the alignment material is removed from the surrounding underfill material to form an interconnect void including the at least one alignment cavity.

23. The process according to claim 16, wherein filling the at least one interconnect void with an interconnect material to form at least one interconnect structure comprises filling the at least one interconnect void with a conductive interconnect material to form at least one conductive interconnect structure.

24. The process according to claim 16, wherein forming at least a first alignment droplet from a flowable alignment material comprises extruding the flowable alignment material through at least a first alignment via to form the at least a first alignment droplet.

25. The process according to claim 24, wherein extruding the flowable alignment material through at least a first alignment via to form at least a first alignment droplet comprises extruding the flowable alignment material through an alignment via located in a reconstruction table.

26. The process according to claim 24, wherein extruding the flowable alignment material through at least a first alignment via to form at least a first alignment droplet comprises extruding the flowable alignment material through an alignment via located in a fixture plate.

27. The process according to claim 16, wherein inducing the at least a first alignment droplet to at least partially solidify and maintain the position of the semiconductor die comprises at least one of raising or lowering a temperature of the alignment material to at least partially solidify the at least a first alignment droplet.

28. The process according to claim 16, wherein inducing the at least a first alignment droplet to at least partially solidify and maintain the position of the semiconductor die comprises reacting the alignment material with an activating agent to at least partially solidify the at least a first alignment droplet.

29. The process according to claim 16, wherein placing a semiconductor die having at least one alignment cavity on a rear surface thereof, such that the at least one alignment cavity of the semiconductor die makes contact with the at least a first alignment droplet and is positioned by the surface tension thereof comprises placing a semiconductor die having a plurality of alignment cavities on the rear surface thereof, each of the alignment cavities of the plurality interacting with a correspondingly positioned alignment droplet to position the semiconductor die.

30. The process according to claim 16, wherein forming at least a first alignment droplet from a flowable alignment material comprises extruding the flowable alignment material through a substrate comprising a fixture plate and introducing an underfill material adjacent the rear surface of the semiconductor die and surrounding the at least a first alignment droplet comprises introducing the underfill material between the semiconductor die and the fixture plate.

31. The process according to claim 30, further comprising curing the underfill material to a substantially solid state.

32. A reconstructed semiconductor wafer comprising:

a plurality of semiconductor dice, each semiconductor die having at least a first alignment via disposed in a rear surface thereof;

a plurality of alignment droplets disposed adjacent the rear surfaces of the plurality of semiconductor dice, each of the at least a first alignment via in contact with a solidified alignment droplet; and

an underfill material disposed adjacent the rear surfaces of the plurality of semiconductor dice and around the alignment droplets.

33. The reconstructed semiconductor wafer of claim 32, further comprising a fixture plate adjacent the plurality of alignment droplets, such that the underfill material is disposed between the rear surfaces of the semiconductor dice and the fixture plate.

34. The reconstructed semiconductor wafer of claim 32, wherein the at least a first alignment via extends from the rear surface of each semiconductor die to an active surface thereof.

35. The reconstructed wafer of claim 34, wherein the at least a first alignment via is filled with a material comprising the alignment droplets.

36. The reconstructed wafer of claim 34, wherein the at least a first alignment via is at least partially filled by a selected filler material.

37. The reconstructed wafer of claim 32, wherein the plurality of alignment droplets comprises a conductive material.

38. A method of performing wafer-level processing on a number of separate semiconductor dice, the method comprising:

selecting a plurality of semiconductor dice;

forming at least one alignment via on a rear surface of each semiconductor die of the plurality;

positioning the semiconductor dice in proper positions to form a semiconductor wafer by placing the at least one alignment via in contact with corresponding alignment droplets positioned on a substrate and using surface tension of the alignment droplets to effect precise alignment of the semiconductor dice;

underfilling the positioned semiconductor dice to form a reconstructed semiconductor wafer; and

performing wafer-level processing on the reconstructed semiconductor wafer.

39. The method of claim 38, wherein selecting a plurality of semiconductor dice comprises selecting a number of known functional dice.

40. The method of claim 38, wherein positioning the semiconductor dice in proper positions to form a semiconductor wafer by placing the at least one alignment via in contact with corresponding alignment droplets further comprises inducing the alignment droplets to at least partially solidify to maintain the proper positions.

41. The method of claim 40, wherein inducing the alignment droplets to at least partially solidify to maintain the proper positions comprises at least one of raising or lowering a temperature of the alignment droplets.

42. The method of claim 38, wherein the substrate comprises a fixture plate and wherein positioning the semiconductor dice in proper positions to form a semiconductor wafer by placing the at least one alignment via in contact with corresponding alignment droplets comprises placing the at least one alignment via in contact with corresponding alignment droplets disposed on the fixture plate.

43. The method of claim 42, wherein underfilling the positioned semiconductor dice to form a reconstructed semiconductor wafer comprises introducing an underfill material between the rear surfaces of the semiconductor dice and a surface of the fixture plate.

44. The method of claim 38, wherein performing wafer-level processing on the reconstructed semiconductor wafer comprises performing a wafer-level testing operation on the reconstructed semiconductor wafer.

45. The method of claim 38, wherein performing wafer-level processing on the reconstructed semiconductor wafer comprises performing burn-in at the wafer level on the reconstructed semiconductor wafer.

46. A reconstruction table comprising:

a platform comprising at least one reconstruction location where at least a first alignment via opens out at a surface of the platform;

a temperature control system for maintaining a desired temperature; and

an alignment material delivery system in communication with the at least a first alignment via, whereby an alignment material may be delivered in a flowable state through the at least a first alignment via to form at least one alignment droplet at the at least one reconstruction location.

47. The reconstruction table of claim 46, wherein the temperature control system includes a temperature-modifying structure selected from the group comprising a resistive heating element, a passageway for circulating fluid within the reconstruction table, and a semiconductor-type heat exchange module.

48. The reconstruction table of claim 46, wherein the temperature control system comprises at least one sensor for monitoring a temperature of the reconstruction table.

49. The reconstruction table of claim 48, wherein the temperature control system further comprises a controller for modulating the temperature of the reconstruction table in response to monitoring by the at least one sensor.

50. The reconstruction table of claim 46, wherein the at least one reconstruction location where at least a first alignment via opens out at the surface of the platform comprises a plurality of alignment vias that open out at the at least one reconstruction location, each of the plurality in communication with the alignment material delivery system.

51. The reconstruction table of claim 46, wherein the platform comprising at least one reconstruction location where at least a first alignment via opens out at the surface of the platform comprises a platform including a plurality of reconstruction locations where at least a first alignment via opens out at the surface of the platform.